PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G06K 19/073, H01L 27/144 — A1

(11) International Publication Number: WO 98/22905

(43) International Publication Date: 28 May 1998 (28.05.98)

(21) International Application Number: PCT/EP97/06168

(22) International Filing Date: 3 November 1997 (03.11.97)

(30) Priority Data:
9624198.9 21 November 1996 (21.11.96) GB

(71) Applicant *(for all designated States except US)*: MOTOROLA LTD. [GB/GB]; Jays Close, Viables Industrial Estate, Basingstoke, Hampshire RG22 4PD (GB).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: WHELAN, John [GB/GB]; 33 Alwyn Drive, East Kilbride G74 4RL (GB). STOUT, Graham, Henry [GB/GB]; 44 Carrick Crescent, Giffnock, Glasgow G46 6PP (GB).

(74) Agents: IBBOTSON, Harry et al.; Motorola, European Intellectual Property Operations, Midpoint, Alencon Link, Basingstoke, Hampshire RG21 7P1 (GB).

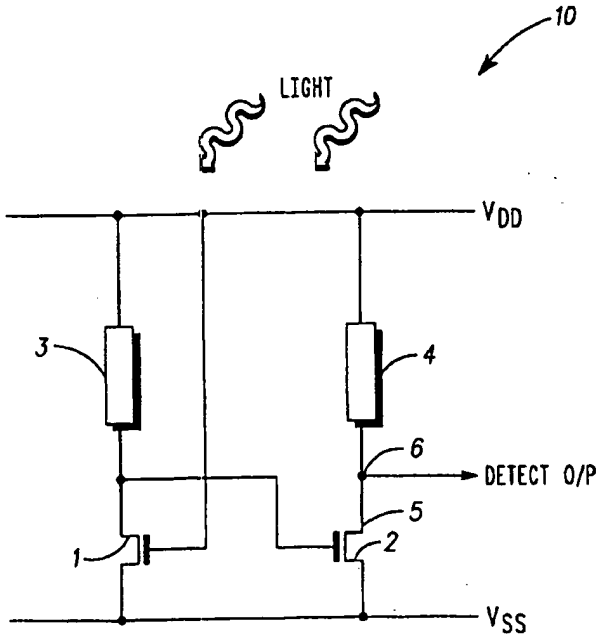
(81) Designated States: CN, JP, US, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: LIGHT DETECTION DEVICE

(57) Abstract

A light detection device has a biasing transistor (1) arranged to provide a bias current and a reverse biased transistor. The reverse biased transistor has a drain terminal (6) coupled via a high impedance resistor (4) to the supply voltage. Incident visible light is detected by a voltage drop at the drain electrode.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece	ML	Mali	TR	Turkey
BG	Bulgaria	HU	Hungary	MN	Mongolia	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MR	Mauritania	UA	Ukraine
BR	Brazil	IL	Israel	MW	Malawi	UG	Uganda
BY	Belarus	IS	Iceland	MX	Mexico	US	United States of America
CA	Canada	IT	Italy	NE	Niger	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NL	Netherlands	VN	Viet Nam
CG	Congo	KE	Kenya	NO	Norway	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NZ	New Zealand	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	PL	Poland		
CM	Cameroon	KR	Republic of Korea	PT	Portugal		
CN	China	KZ	Kazakstan	RO	Romania		
CU	Cuba	LC	Saint Lucia	RU	Russian Federation		
CZ	Czech Republic	LI	Liechtenstein	SD	Sudan		
DE	Germany	LK	Sri Lanka	SE	Sweden		
DK	Denmark	LR	Liberia	SG	Singapore		
EE	Estonia						

LIGHT DETECTION DEVICE

Field of the Invention

This invention relates to light detection devices and particularly but not exclusively to light detection devices for use in tamper detection applications.

Background of the Invention

In a semiconductor integrated circuit (IC), such as a banking smartcard, the IC is vulnerable to a breach of security if it falls into the hands of a dishonest person. The IC may be reverse engineered in order to reveal or modify functions and confidential data contained therein. It is known that such IC's have been decapsulated and have even undergone depassivation of the upper protective layer.

US patent 4,952,796 describes a circuit which comprises a current generator delivering current which flows into a reversed biased transistor junction. If subject to light, the reverse current in the junction increases, and the voltage at the junction terminals drops.

A problem with this arrangement is that incident light will generate reverse currents in transistors 11 and 2 of FIG.1, and this may affect the voltage drop detected at the output. Furthermore, the biasing and current generation functions of the above circuit are more susceptible to manufacturing process variations.

Also current drain, particularly in a smartcard, should be kept to a minimum, and the reverse current adversely affects the current consumption of the device. Lastly, the above circuit takes up much valuable semiconductor area, and again this is disadvantageous in a smartcard, where demand for space is at a premium.

This invention seeks to provide a light detection device which mitigates the above mentioned disadvantages.

Summary of the Invention

According to the present invention there is provided a light detection device comprising: a biasing transistor, arranged to provide a bias current; a reverse biased transistor having a control electrode arranged to be reverse biased by the bias current and having a conducting electrode; and, a resistor coupled between a supply voltage and the conducting electrode of the reverse biased transistor; wherein incident visible light is detected by a voltage drop at the conducting electrode of the reverse biased transistor.

In this way a light detection device is provided which does not generate parasitic reverse currents, and is less susceptible to manufacturing process variations.

Brief Description of the Drawing(s)

An exemplary embodiment of the invention will now be described with reference to the single figure drawing which shows a preferred embodiment of a light detection device in accordance with the invention.

Detailed Description of a Preferred Embodiment

Referring to the single figure drawing, there is shown a light detection device 10, arranged to be integrated with an IC.

The device 10 comprises a first transistor 1, having a gate terminal coupled to a supply voltage Vdd, a source terminal coupled to a ground terminal Vss and a drain terminal coupled to the supply voltage Vdd via a first high impedance resistor 3. The first transistor 1 is thus arranged to provide a bias current to be further described below.

A second transistor 2 of the device 10 has a gate terminal coupled to the drain terminal of the first transistor 1, a source terminal coupled to the ground terminal Vss and a drain terminal 5 coupled to the supply voltage

Vdd via a second high impedance resistor 4, and further coupled to an output terminal 6. The high impedance resistor 4 is an undoped polysilicon resistor.

In operation, the gate terminal of the second transistor 2 is arranged to be reverse biased by receiving the bias current from the drain terminal of the first transistor 1.

When the drain terminal 5 of the second transistor is subjected to incident visible light, a small reverse current is generated between drain 5 and the ground terminal Vss. This current flow lowers the voltage at drain 5, and this voltage drop is detected by circuitry (not shown) coupled to the output terminal 6.

Since the second high impedance resistor is an undoped polysilicon resistor, extremely small currents can be detected, making the device 10 very sensitive to incident light.

No parasitic reverse currents are generated, and during the manufacturing process of the device 10, only one resistivity process is required to fabricate the first and the second high impedance resistors 3 and 4, and this will not introduce variations which will significantly affect the performance of the device 10.

It will be appreciated that alternative embodiments to the one described above are possible. For example, the biasing arrangement may vary from the precise configuration described above. In addition, the first and second resistors could be fabricated from a material other than undoped polysilicon.

Claims

1. A light detection device comprising:
a biasing circuit arranged to provide a bias current;
a reverse biased transistor having a control electrode arranged to be reverse biased by the bias current and having a conducting electrode; and,
a resistor coupled between a supply voltage and the conducting electrode of the reverse biased transistor;
wherein incident visible light is detected by a voltage drop at the conducting electrode of the reverse biased transistor.

2. The device of claim 1 wherein the resistor is a high impedance resistor.

3. The device of claim 1 wherein the resistor is an undoped polysilicon resistor.

4. The device of claim 1 wherein the biasing circuit comprises a biasing transistor having a conducting electrode coupled to the supply voltage via a biasing resistor.

5. The device of claim 4 wherein the biasing resistor is a high impedance resistor.

6. The device of claim 5 wherein the biasing resistor is an undoped polysilicon resistor.

7. A smart-card incorporating the device of claim 1.

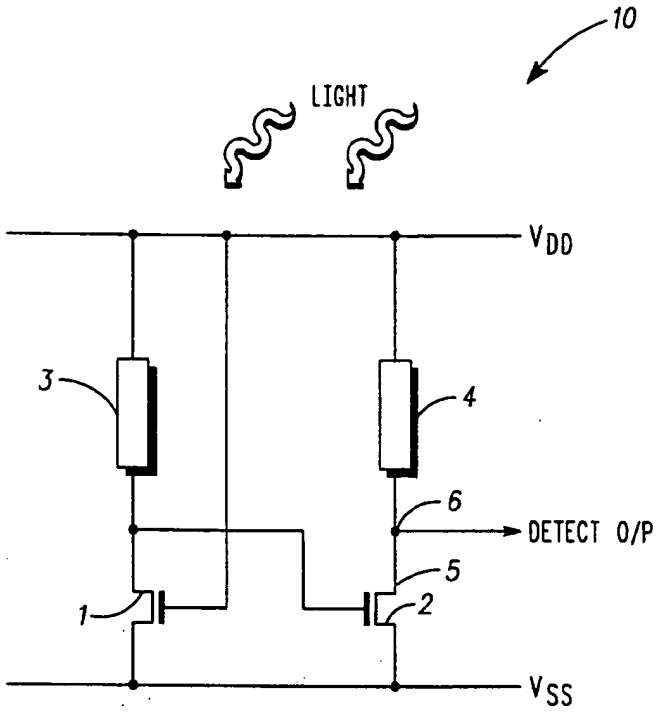


FIG.1

INTERNATIONAL SEARCH REPORT

Inter onal Application No
PCT/EP 97/06168

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06K19/073 H01L27/144

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06K H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4 952 796 A (FRUHAUF SERGE ET AL) 28 August 1990 cited in the application see abstract; figure 1	1-7
A	GB 2 074 788 A (TOKYO SHIBAURA ELECTRIC CO) 4 November 1981 see abstract; figures 3,5 see page 1, line 38 - line 52 see page 2, line 3 - line 15	1-6
A	US 4 910 707 A (SCHRENK HARTMUT) 20 March 1990 see figures 2,4 see column 3, line 23 - column 4, line 24	1-6

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 April 1998	22/04/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Visscher, E

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Inter onal Application No
PCT/EP 97/06168

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 437 307 A (PARADIGM TECHNOLOGY INC) 17 July 1991 see abstract; figure 2 see column 2, line 2 - line 32	1-3

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter[illegible]onal Application No
PCT/EP 97/06168

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4952796 A	28-08-90	FR 2619959 A	03-03-89
		DE 3875431 A	26-11-92
		EP 0306395 A	08-03-89
		JP 1091022 A	10-04-89
GB 2074788 A	04-11-81	JP 56150871 A	21-11-81
		DE 3115695 A	04-02-82
		US 4949152 A	14-08-90
US 4910707 A	20-03-90	EP 0178512 A	23-04-86
		JP 61084054 A	28-04-86
EP 0437307 A	17-07-91	US 5172211 A	15-12-92
		CA 2034057 A	13-07-91
		JP 5267581 A	15-10-93
		US 5168076 A	01-12-92

Form PCT/ISA/210 (patent family annex) (July 1992)